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Docket No. 20063/10014

"EXPRESS MAIL" mailing label No.
EL 995 292 941 US
Date of Deposit: **December 29, 2003**

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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Dae Kyeun KIM**, a citizen of the Republic of Korea, residing at #106-102 Singal Hanshin Apt., Singal-ri, Giheung-eup, Yongin-si, Gyeonggi-do, 449-907, Korea have invented a new and useful **METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES**, of which the following is a specification.

METHODS OF MANUFACTURING SEMICONDUCTOR DEVICES

TECHNICAL FIELD

[0001] The present disclosure relates to semiconductors and, more particularly, to method of manufacturing semiconductor devices.

BACKGROUND

[0002] Generally, in the manufacture of semiconductor devices, a transistor is fabricated according to following steps. First, a gate electrode is formed on a substrate and a source/drain region with shallow junction is formed through an ion implantation process using the gate electrode as a mask. Next, spacers are formed on sidewalls of the gate electrode and a source/drain region with deep junction is formed through an ion implantation using the spacers as a mask. As a result, a transistor comprising the gate electrode and an expanded source/drain region is formed in the substrate. The expanded source/drain region consists of the source/drain region with shallow junction as the lightly doped drain (LDD) region and the source/drain region with deep junction. Next, to reduce resistance during electrical operation of the transistor, a silicide layer is formed on the gate electrode and the surface of the substrate including the source/drain region. Here, the silicide layer is not formed on the spacers.

[0003] A prior approach is disclosed in U.S. Patent No. 5,918,130 to Hause et al. that discloses a method for fabricating a transistor employing formation of silicide across a source/drain region prior to formation of the gate conductor. In particular, dopants are forwarded into a lateral region of a substrate to form an implant region. Then, a silicide layer and a sacrificial layer are formed respectively. A contiguous opening is formed through the sacrificial layer and the silicide layer, exposing a portion of the substrate. Dopants are then implanted into the exposed substrate region to form a channel. Spacers are formed on opposed sidewall surfaces of the sacrificial layer within the opening. A gate oxide is then formed across the exposed region, followed by the formation of a polysilicon gate conductor across the gate oxide. A polycide is formed across the gate conductor before the sacrificial layer is removed.

[0004] An alternate prior approach is disclosed in U.S. Patent No. 6,087,235 to Yu, which discloses a method for fabricating a field effect transistor with elevated source/drain contact structures. A field effect transistor includes a drain extension implant, a source extension implant, a gate dielectric, a gate structure disposed over the gate dielectric, and a first spacer disposed on sidewalls of the gate dielectric and of the gate structure. An elevated drain contact structure is selectively grown on the drain extension implant and has a drain facetted surface facing toward the first spacer on the sidewall of the gate structure. Similarly, an elevated source contact structure is selectively grown on the source extension implant and has a source facetted surface facing toward the first spacer on the sidewall of the gate structure. A second spacer is formed to cover the drain facetted surface and the source facetted surface before dopant implantation into and silicide formation on the elevated drain and source contact structures.

[0005] Figs. 1a through 1k illustrate, in cross-sectional views, the results of process steps for manufacturing a semiconductor device according to a known method.

[0006] Referring to Fig. 1a, a gate oxide layer 12 and a gate poly layer 14 are formed on a substrate 10 and a mask pattern 15 is formed over the gate poly layer 14.

[0007] Referring to Fig. 1b, the gate oxide layer 12 and the gate poly layer 14 are etched using the mask pattern 15 as an etching mask to form a gate electrode 16 comprising a gate poly pattern 14a and a gate oxide pattern 12a.

[0008] As shown in Fig. 1c, an ion implantation is performed using the gate electrode 16 as a mask to form a source/drain region 18 with shallow junction adjacent to the gate electrode 16 in the substrate 10.

[0009] Referring to Fig. 1d, an insulating layer is deposited over the substrate 10 including the gate electrode 16. Then, an etch back process is performed for the insulating layer to form spacers 20 on sidewalls of the gate electrode 16.

[0010] Referring to Fig. 1e, an ion implantation is performed using the spacers 20 as a mask to form a source/drain region 22 with deep junction adjacent to the spacers 20 in the substrate 10. As a result, an expanded source/drain region 24 with an LDD region is formed in the substrate 10.

[0011] With reference to Fig. 1f, a metal layer 26 is formed over the substrate 10 including the gate electrode 16 and the spacers 20. The metal layer 26 is a multi-layer consisting of a titanium layer and a titanium nitride layer.

[0012] Referring to Fig. 1g, a first thermal treatment process is performed for the substrate 10 including the metal layer 26. By the thermal treatment, salicidation reaction occurs. As a result, a preliminary silicide layer 28a is formed on top of the gate electrode 16 and the surface of the substrate 10 including the source/drain region 24. However, the salicidation reaction does not occur in the metal layer 26 on the spacers 20 and, therefore, the preliminary silicide layer 28a is not formed on the spacers 20. The metal layer 26 unchanged on the spacers 20 is removed.

[0013] Referring to Fig. 1h, a second thermal treatment process is performed for the substrate 10 including the preliminary silicide layer 28a. As a result, the preliminary silicide layer 28a is changed into a silicide layer 28.

[0014] Referring to Fig. 1i, an insulating layer pattern 30 with contact holes 30a is formed over the substrate 10 including the silicide layer 28. Through the contact holes 30a, the silicide layer 28 on the gate electrode and some part of the silicide layer 28 on the substrate 10 including the source/drain region 24 are exposed.

[0015] Referring to Figs. 1j and 1k, a barrier metal layer 32 is formed on bottom and sidewalls of the contact holes 30a. Then, the contact holes 30a are filled with conductive material and an etch back process is performed to form contact plugs.

[0016] Here, the spacers function as a mask for ion implantation. In addition, the silicide layer is not formed on the spacers. Such spacers are a necessary structure in manufacturing a semiconductor device but are unnecessary in respect of device operation. Particularly, the spacers may cause leakage during device operation. To obviate these shortcomings, a process omitting formation of the spacers has been developed. However, such a conventional method may increase electrical resistance in a device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Figs. 1a through 1k illustrate, in cross-sectional views, results of the process steps for fabricating a semiconductor device according to a known method.

[0018] Figs. 2a through 2j illustrate, in cross-sectional views, results of example disclosed process steps for fabricating a semiconductor device.

DETAILED DESCRIPTION

[0019] Referring to Fig. 2a, a gate oxide layer 42 and a gate poly layer 44 are formed in sequence on a substrate 40. A mask layer 46 is formed over the gate poly layer 44. The mask layer 46 is preferably a photoresist pattern formed by photolithography.

[0020] As shown in Fig. 2b, an etching process is performed using the mask layer 46 as an etching mask to form a gate poly pattern 44a and a gate oxide pattern 42a. The mask layer 46 is removed. As a result, a gate electrode 48 comprising the gate oxide pattern 42a and the gate poly pattern 44a is formed on the substrate 40.

[0021] Referring to Fig. 2c, an ion implantation process is performed using the gate electrode 48 as a mask. As a result, a first preliminary source/drain region 50 with shallow junction is formed adjacent to the gate electrode 48 in the substrate 40.

[0022] Referring to Fig. 2d, a nitride layer 52 is formed on the substrate 40 including the gate electrode 48. The nitride layer 52 is preferably about 300Å in thickness and is formed to ensure a margin for misalign when an ILD pattern with contact holes is formed in a following process.

[0023] Referring to Fig. 2e, an ILD pattern 54 with contact holes 54a is formed over the substrate 40. Through the contact holes 54a, the top of the gate electrode 48 and some part of the first preliminary source/drain region 50 are exposed. In particular, an ILD is formed on the substrate 40. The ILD may be formed of borophosphosilicate glass (BPSG) or tetraethyl orthosilicate (TEOS) and may be a single layer or a multi-layer. Then, a planarization process such as chemical mechanical polishing (CMP) is performed to flatten the surface of the ILD. Then, a photoresist pattern is formed on the ILD. An etching process is performed using the photoresist pattern as an etching mask to form an ILD pattern 54 with contact holes 54a.

[0024] Referring to Fig. 2f, an ion implantation process is performed using the ILD pattern 54 as a mask to implant ions into the parts exposed through the contact holes

54a. By the ion implantation, a second preliminary source/drain region 56 with deep junction is formed in the substrate 40. As a result, an expanded source/drain region 58 with an LDD region is formed in the substrate 40. The expanded source/drain region includes the first preliminary source/drain region 50 and the second preliminary source/drain region 56. In addition, the ion implantation results in an increase of doping concentration in the gate electrode 48. Therefore, electric resistance of the gate electrode 48 can be reduced due to such an increase of doping concentration.

[0025] Referring to Fig. 2g, the ion implantation process may be continuously performed until the parts exposed through the contact holes 54a have a single crystal structure.

[0026] Referring to Fig. 2h, a barrier metal layer 60 is formed on sidewalls and bottoms of the contact holes 54a. The barrier metal layer 60 may be formed of titanium, titanium nitride, or cobalt. Alternatively, the barrier metal layer 60 a multi-layer structure comprising a titanium layer and a titanium nitride layer or a cobalt layer, a titanium layer and a titanium nitride layer.

[0027] Referring to Fig. 2i, a silicide layer 62 is formed on the bottoms of the contact holes 54a through thermal treatment of the substrate 40. The silicide layer 62 is formed using the barrier metal layer 60. In one example, the formation of the barrier metal layer 60 may be omitted. Therefore, if the barrier metal layer is not formed in the contact holes 54a, a metal layer is deposited only on the bottoms of the contact holes 54a to form the silicide layer 62 through a thermal treatment process. Here, the metal layer may be formed of titanium, titanium nitride, or cobalt. Alternatively, the metal layer may be a multi-layer structure comprising a titanium layer and a titanium nitride layer or a cobalt layer, a titanium layer, and a titanium nitride layer. Thus, to simplify the process, the silicide layer 62 may be formed using the barrier metal layer 60.

[0028] The process for forming the silicide layer 62 is now described in detail. First, a metal layer is formed on the top of the gate electrode 48 and the surface of the substrate 40 including the expanded source/drain region 58. A first thermal treatment process is performed for the substrate 40 including the metal layer. Then, a second

thermal treatment process is performed for the substrate 40 in situ. As a result, the metal layer is changed into the silicide layer 62 by salicidation reaction. In one example, the metal layer may be the barrier metal layer 60.

[0029] In one example, if the metal layer for the formation of the silicide layer 62 is a multi-layer comprising a titanium layer and a titanium nitride layer, the titanium layer may be about 300 Å in thickness and the titanium nitride layer may be about 150 Å in thickness. In addition, in case of the metal layer comprising the titanium layer and the titanium nitride layer, the first thermal treatment may be performed using a nitrogen gas for about 30 seconds at temperature of about 720 ℃ and the second thermal treatment may be performed using a nitrogen gas for about 20 seconds at temperature of about 820℃.

[0030] According to another example, if the metal layer for the formation of the silicide layer 62 is a multi-layer comprising a cobalt layer, a titanium layer, and a titanium nitride layer, the cobalt layer, the titanium layer, and the titanium nitride layer may be about 150 Å, 100 Å, and 150 Å in thickness, respectively. In addition, in case of the metal layer comprising the cobalt layer, the titanium layer, and the titanium nitride layer, the first thermal treatment may be performed using a nitrogen gas for a time between about 50 seconds and 70 seconds at a temperature between about 460℃ and 500℃. The second thermal treatment may be performed using a nitrogen gas for a time between about 25 seconds and 35 seconds at a temperature between about 800℃ and 840℃.

[0031] Referring to Fig. 2j, the contact holes 54a are filled with conductive material to form contact plugs 64. The conductive material may be, for example, tungsten material that has good filling properties. In particular, the conductive material is deposited over the ILD pattern 54 and in the contact holes 54a. A planarization process such as CMP is performed until the surface of the ILD pattern 54 is exposed. As a result, the conductive material remains in the contact holes 54a to form the contact plugs 64.

[0032] Next, a metal interconnect is formed over the ILD pattern 54 including the contact plugs 64. Thus, the contact plugs 64 are electrically connected by the metal interconnect.

[0033] As disclosed herein, a semiconductor device may include an LDD region and a silicide layer without spacers. In addition, the present invention can improve operation characteristics as well as electrical characteristics of device in manufacturing semiconductor devices such as SRAM.

[0034] As disclosed herein, one example method of manufacturing a semiconductor device includes forming a gate electrode on a substrate, forming a first preliminary source/drain region with shallow junction in the substrate by performing ion implantation using the gate electrode as a mask, and forming an interlayer dielectric (ILD) pattern with contact holes over the substrate including the gate electrode and the first preliminary source/drain region, the contact holes exposing the top of the gate electrode and some part of the first preliminary source/drain region. The example method may further include forming an expanded source/drain region by performing an ion implantation using the ILD pattern as a mask, the expanded source/drain region including the first preliminary source/drain region with shallow junction as the LDD region and a second preliminary source/drain region with deep junction, forming a silicide layer on the top of the gate electrode and the expanded source/drain region and forming contact plugs by filling the contact holes with metal.

[0035] An alternate example method may include forming a nitride layer with a thickness between 250 Å and 350 Å over the substrate including the gate electrode; and forming a barrier metal layer on sidewalls and bottoms of the contact holes.

[0036] The silicide layer may be formed by forming a metal layer on the top of the gate electrode and the surface of the substrate including the expanded source/drain region, performing a first thermal treatment process for the substrate including the metal layer, and performing a second thermal treatment process in situ for the resulting substrate.

[0037] The metal layer for formation of the silicide layer is preferably formed of one selected form the group consisting of titanium, titanium nitride, and cobalt.

[0038] According to another example, the metal layer for formation of the silicide layer may be a multi-layer consisting of a titanium layer and a titanium nitride layer. The titanium layer may be between 250Å and 350Å in thickness. Alternatively, the titanium nitride layer may be between 100Å and 200Å in thickness. The first thermal treatment may be performed using a nitrogen gas for a time between 25 seconds and 35 seconds at a temperature between 700℃ and 740℃. The second thermal treatment may be performed using a nitrogen gas for a time between 15 seconds and 25 seconds at a temperature between 800℃ and 840℃.

[0039] The metal layer for formation of the silicide layer may be a multi-layer consisting of a cobalt layer, a titanium layer, and a titanium nitride layer. Alternatively, the cobalt layer may be between 120 Å and 170 Å in thickness. The titanium layer may be 80Å and 120 Å in thickness. The titanium nitride layer may be 130 Å and 170 Å in thickness. The first thermal treatment may be preformed using a nitrogen gas for a time between 50 seconds and 70 seconds at a temperature between 460 °C and 500 °C. The second thermal treatment may be performed using a nitrogen gas for a time between 25 seconds and 35 seconds at a temperature between 800 °C and 840 °C.

[0040] In any of the foregoing embodiments, the contact plugs may be tungsten and a metal interconnect deposited over the ILD pattern including the contact plugs may be formed of aluminum.

[0041] Although certain example methods are disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.